WE CLAIM:

1. Apparatus for processing data, said apparatus comprising:

an data processing circuit operable to perform data processing;

a diagnostic interface circuit coupled to said data processing circuit and operable to perform diagnostic operations upon said data processing circuit, said data processing circuit being switchable between a first state in which said diagnostic interface circuit cannot perform at least some diagnostic operations upon said data processing circuit and a second state in which said diagnostic interface circuit can perform said at least some diagnostic operations upon said data processing circuit; and

a diagnostic transaction request master circuit coupled via a diagnostic transaction bus to said diagnostic interface circuit and operable to issue diagnostic transaction requests to said diagnostic interface circuit; wherein

said diagnostic interface circuit is responsive to a diagnostic transaction request received from said diagnostic transaction request master whilst said data processing circuit is in said first state to return a diagnostic bus transaction error signal to said diagnostic transaction request master.

2. Apparatus as claimed in claim 1, wherein said data processing circuit is in a low power consumption state whilst in said first state and said data processing circuit is in an operational state whilst in said second state.

3. Apparatus as claimed in claim 2, wherein said diagnostic interface circuit remained powered whilst said data processing circuit is in said first state.

4. Apparatus as claimed in claim 1, comprising a plurality of data processing circuits having respective diagnostic interface circuits and coupled to said diagnostic transaction request master via said diagnostic transaction bus.

5. Apparatus as claimed in claim 1, wherein said diagnostic interface circuit is operable to continue to return a diagnostic bus transaction error signal to said diagnostic transaction request master following said data processing circuit switching

between said second state and said first state until a request is made to clear generation of said diagnostic bus transaction error signal.

6. Apparatus as claimed in claim 5, wherein said diagnostic interface circuit includes a state change detecting circuit operable to set a state change indicating latch within said diagnostic interface upon detection of said data processing circuit changing between said second state and said first state, said state change indicating latch being reset when said diagnostic transaction request master requests clearing of diagnostic bus transaction signal generation, and said bus interface circuit being operable to generate a diagnostic bus transaction error signal in response to a diagnostic transaction request when said state change indicating latch is set.

7. Apparatus as claimed in claim 1, comprising a system-on-chip integrated circuit.

8. A method of processing data, said method comprising the steps of:

performing data processing with a data processing circuit;

performing diagnostic operations upon said data processing circuit with a diagnostic interface circuit coupled to said data processing circuit, said data processing circuit being switchable between a first state in which said diagnostic interface circuit cannot perform at least some diagnostic operations upon said data processing circuit and a second state in which said diagnostic interface circuit can perform said at least some diagnostic operations upon said data processing circuit; and

issuing diagnostic transaction requests to said diagnostic interface circuit with a diagnostic transaction request master circuit coupled via a diagnostic transaction bus to said diagnostic interface circuit; wherein

in response to a diagnostic transaction request received whilst said data processing circuit is in said first state, returning a diagnostic bus transaction error signal.

9. A method as claimed in claim 8, wherein said data processing circuit is in a low power consumption state whilst in said first state and said data processing circuit is in an operational state whilst in said second state.

10. A method as claimed in claim 9, wherein said diagnostic interface circuit remained powered whilst said data processing circuit is in said first state.

11. A method as claimed in claim 8, comprising a plurality of data processing circuits having respective diagnostic interface circuits and coupled to said diagnostic transaction request master via said diagnostic transaction bus.

12. A method as claimed in claim 8, wherein said diagnostic interface circuit is operable to continue to return a diagnostic bus transaction error signal to said diagnostic transaction request master following said data processing circuit switching between said second state and said first state until a request is made to clear generation of said diagnostic bus transaction error signal.

13. A method as claimed in claim 12, wherein said diagnostic interface circuit includes a state change detecting circuit operable to set a state change indicating latch within said diagnostic interface upon detection of said data processing circuit changing between said second state and said first state, said state change indicating latch being reset when said diagnostic transaction request master requests clearing of diagnostic bus transaction signal generation, and said bus interface circuit being operable to generate a diagnostic bus transaction error signal in response to a diagnostic transaction request when said state change indicating latch is set.

14. A method as claimed in claim 8, comprising a system-on-chip integrated circuit.